Remarks:

The examiner and his supervisor are thanked for the interview of September 20, 2005 in which 102 rejection over Ker and the 112 rejection were discussed.

Claim Rejections – 35 USC 112

Claims 2 has been amended to avoid section 112 issues.

Claim 2 now specifies that the p-n junction is between the p-well and p+region on the one hand, and the n+ region on the other hand. This provides for a p-n junction while avoiding the need for the p+ region and n+ region to be physically touching each other.

Claim 3 avoids this problem altogether by simply defining a forward biased diode in the p-well. Since the n+ regions and p+ regions in the p-well are not isolated but allow current flow through the p-well, the n+ region and p+ region/p-well again define a diode that is forward biased.

Claim Rejections – 35 USC 102

Claims 2-4 and 6 were rejected under 35 USC 102 over Ker.

As discussed during the interview, the claims explicitly require a p-well with an n+ region and a p+ region, and forming at least one additional n+ region and at least one additional p+ region in the p-well. Thus there have to be at least two n+ regions and at least two p+ regions in the p-well. Furthermore the p-n junctions or diodes formed in the p-well have to be forward biased. This has been further defined in claim 2 by stating that for the diode the p+ region is located on the high voltage side of the n+ region.

In contrast Ker shows two types of structures: an NMOS triggered LVTSCR (Figure 3A) and a PMOS triggered LVTSCR (Figure 4A). The examiner argued that Figures 6 show a PMOS triggered LVTSCR connected to an NMOS triggered LVTSCR and that it would be obvious to provide the connections between the two structures internally.

Figures 6 of Ker show the cathode of the PMOS triggered LVTSCR connected to the anode of the NMOS triggered LVTSCR. This would provide a structure as shown in the attached Figure A. This therefore still does not provide a p-well with at least to n+regions and at least two p+ regions since this configuration would provide n-well, followed by p-well, followed by n-well, followed by p-well.

Even if the NMOS triggered LVTSCR were turned around so that the cathode of the NMOS triggered LVTSCR and the cathode of the PMOS triggered LVTSCR were connected together (which is nowhere shown or suggested in Ker), the resultant n-well and double p-well would be as shown in attached Figure B. The NMOS triggered LVTSCR side of this structure (anode on the left hand side with the low voltage side being on the right hand side) would still not provide forward biased diodes in the p-well since it has all the n+ regions on the high voltage or anode side of the p-regions. The only regions where the p+ region is on the high voltage side of a n+ region are the regions that are connected together as cathode and are therefore shorted out and cannot define a diode. Thus, not only is the connection of Figure B not taught or suggested by Ker, it also does not provide for the required forward biased diodes in the p-well.

Thus all of the claims distinguish over Ker and avoid any ambiguity. Early allowance of the claims as they now stand is therefore respectfully requested.

Respectfully Submitted,

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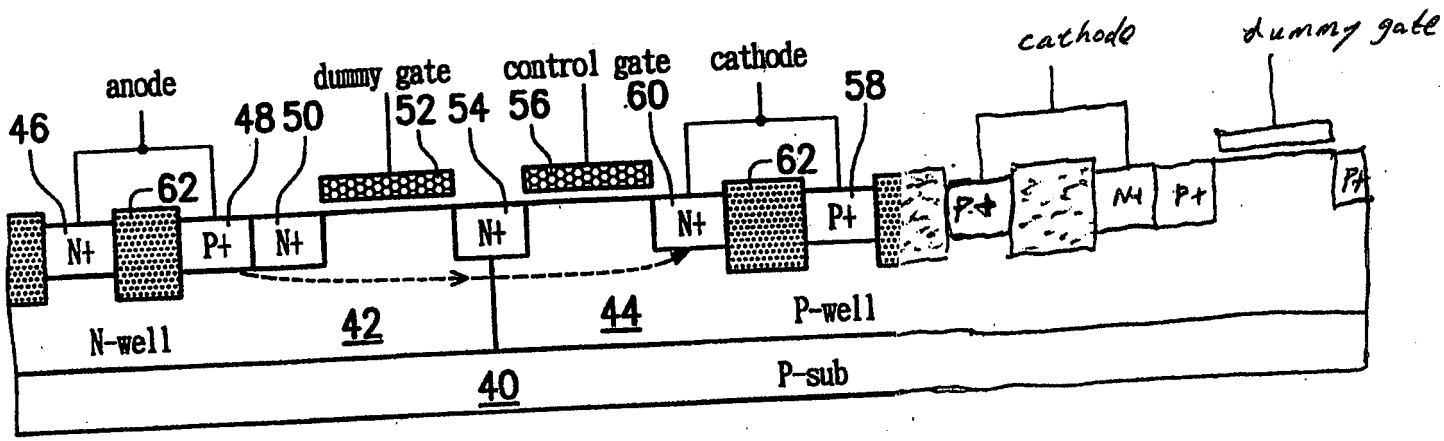
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Fig 8